

WHAT IS CLAIMED IS:

- 1           1. A via for use in a printed circuit board having a circuit, the via  
2 comprising:  
3               a first interconnect; and  
4               a second interconnect located about at least a portion of the first  
5 interconnect, the second interconnect being coaxial with the first interconnect and  
6 inductively coupled with the first interconnect, the second interconnect being  
7 connected to ground of the circuit.
- 1           2. The via of claim 1, wherein the first and second interconnects are  
2 substantially concentric.
- 1           3. The via of claim 2, wherein the first and second interconnects are  
2 cylinders in a single via hole.
- 1           4. The via of claim 1, wherein the second interconnect is operatively  
2 connected to at least two layers of the printed circuit board.
- 1           5. The via of claim 1, wherein a series ground inductance present in the  
2 signal return path is essentially canceled.
- 1           6. The via of claim 1, wherein the signal return has a voltage drop that  
2 approaches zero.
- 1           7. The via of claim 4, where the layers are located in a single printed  
2 circuit board.

1           8. The via of claim 4, where the layers are located in a monolithically  
2 integrated set of two or more printed circuit boards.

1           9. A printed circuit board comprising:  
2 a plurality of vias according to claim 1.

1           10. A method of electrically interconnecting multiple layers on a printed  
2 circuit board to provide a common ground plane for a circuit, the method  
3 comprising:  
4           connecting a first layer and at least a second layer to a via disposed in  
5 a through-hole of a printed circuit board, the via comprising a first interconnect  
6 and a second interconnect located about at least a portion of the first interconnect,  
7 the second interconnect being coaxial and substantially concentric with the first  
8 interconnect and inductively coupled with the first interconnect, the second  
9 interconnect being connected to ground of the circuit.

1           11. The method of claim 10, wherein at least two layers on a printed  
2 circuit board connect to the second interconnect to form one signal reference.

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